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The thermoelectric properties of Ge/SiGe modulation doped superlattices

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The thermoelectric and physical properties of superlattices consisting of modulation doped Ge quantum wells inside Si_{1-y}Ge_y barriers are presented, which demonstrate enhancements in the thermoelectric figure of merit, ZT , and power factor at room temperature over bulk Ge, Si_{1-y}Ge_y, and Si/Ge superlattice materials. Mobility spectrum analysis along with low temperature measurements indicate that the high power factors are dominated by the high electrical conductivity from the modulation doping. Comparison of the results with modelling using the Boltzmann transport equation with scattering parameters obtained from Monte Carlo techniques indicates that a high threading dislocation density is also limiting the performance. The analysis suggests routes to higher thermoelectric performance at room temperature from Si-based materials that can be fabricated using micro- and nano-fabrication techniques. © 2013 AIP Publishing LLC.

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I. INTRODUCTION

Thermoelectric generators use the Seebeck effect to convert thermal energy into electrical energy. Since waste heat is abundant, there is renewed interest in thermoelectrics for a range of applications including industrial energy harvesting,¹ replacing car alternators to improve automotive fuel consumption to powering autonomous, remote sensors.^{2,3} The major use of thermoelectric materials is as heat pumps for cooling applications where the Peltier effect uses an electrical current to pump heat. Every telecoms laser is thermally controlled by a Peltier cooler to maintain the temperature within 0.1 °C thereby providing stable output wavelengths for communications.⁴

There are two figures of merit which are important in defining the performance of thermoelectric materials. The first is

$$ZT = \frac{\alpha^2 \sigma}{\kappa} T, \quad (1)$$

in which α is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the temperature.⁴ The second is the power factor which is equal to $\alpha^2 \sigma$. Both are important for the design of practical devices as the maximum thermodynamical efficiency for converting thermal into electrical energy between a hot source (T_H) and a cold sink (T_C) is given by⁴

$$\eta_{max} = \frac{T_H - T_C}{T_H} \frac{\sqrt{1 + ZT} - 1}{\sqrt{1 + ZT} + \frac{T_C}{T_H}}, \quad (2)$$

where T is the median of T_H and T_C . The first term on the right hand side of the equation is the Carnot efficiency whilst the second term corresponds to Joule losses and other irreversible processes that result in additional loss mechanisms that lower efficiency. The other important design parameter to optimize material is the maximum power that can be generated for a thermoelectric generator placed in a system with perfect heat sinking which is given by⁵

$$P_{max} = \frac{1}{2} FN \frac{A}{L} \Delta T^2 \alpha^2 \sigma, \quad (3)$$

in which F is the fabrication factor, N is the number of legs in the thermoelectric module, A is the area of the legs, L is the length of the legs, and $\Delta T = T_H - T_C$.

The majority of thermoelectric generators and Peltier coolers aimed for applications close to room temperature are fabricated from Bi₂Te₃ and the alloy Bi₂Te_{1-x}Sb_x.^{4,6} SiGe alloys have been used for high temperature thermoelectrics (up to 900 °C),⁷ especially for radioisotope thermoelectric generators, but the ZT and power factor values previously demonstrated at room temperature are significantly lower than those of Bi₂Te₃. As tellurium is one of the rarest elements on earth, there is significant interest in removing tellurium from thermoelectric materials and replacing it with more sustainable materials. SiGe alloys are sustainable and also have the advantage of being able to be processed in semiconductor foundries. Micro ElectroMechanical System (MEMS) microfabrication can therefore be used to produce thermoelectric generators and Peltier coolers potentially allowing cheap and reliable manufacturing routes along with the ability to integrate the thermoelectrics on silicon chips to allow on-chip-cooling or energy harvesting.

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A good thermoelectric material should be a good electrical conductor but also a good thermal insulator. This condition is difficult to meet in bulk three dimensional (3D) structures since the electrical and thermal conductivities of electron and hole gases are linked by the Wiedemann–Franz law which provides a fundamental limit to the maximum ZT attainable in thermoelectric devices made from bulk materials. Whilst Whall and Parker first suggested the use of low dimensional Si/SiGe heterostructures for enhancing thermoelectrics,⁸ the first theoretical work to investigate low dimensional structures was undertaken by Hicks and Dresselhaus.^{9,10} The discontinuities in the density of states for low dimensional structures produces an asymmetry around the chemical potential which enhances the Seebeck coefficient.¹¹ In the two-dimensional (2D) systems, the quantum wells (QWs) also allow enhancements to the electrical conductivity through higher mobility from modulation doping.^{12–14} The use of quantum or nanoscale structures can also provide modifications to the phonon and thermal conductivity properties of materials and devices, and significant reductions to the thermal conductivities over bulk materials have been reported for 2D, 1D, and 0D nanostructures.¹⁵

Previous work on SiGe alloys and Si/Ge superlattices (SLs) has been predominantly related to the n-type material. For high temperature applications, the best n-SiGe alloys have a $ZT \sim 1$ at between 900 and 950 °C (Ref. 7), but the ZT of p-type material has remained much lower, with the best results around 0.65 (Ref. 7). Recent work on nanostructured particles inside a SiGe matrix have now demonstrated improved ZT s of 0.95 in the p-type material at 800 °C and $ZT = 1.3$ at 900 °C.^{16,17} At room temperature, the ZT values reported for both n- and p-type SiGe materials are significantly lower with values well below 0.1 (Ref. 7, see Table I for comparisons of literature values). Whilst there have been a significant number of publications investigating the thermal conductivity of Si/Ge and Si/SiGe superlattices,^{18–21} there are far fewer publications investigating doped superlattices with sufficient results to quote ZT , power factors, or the output from a cooler.^{22–24} To date these reported results for Si/Ge and Si/SiGe superlattices are only for n-type material

(Ref. 23) where the room temperature ZT was 0.004 which is well below the theoretically predicted value of 0.96.²⁵

In this paper we investigate p-type Ge/SiGe modulation doped superlattices for in-plane thermoelectric generation for the first time and investigate the properties as a function of QW width for samples with two different $\text{Si}_{1-x}\text{Ge}_x$ concentrations. For in-plane transport, both the electrical and thermal conductivity is parallel to the barriers and along the QWs. A Hall bar has been fabricated with integrated heaters, thermometers, and electrical probes to allow the electrical conductivity, thermal conductivity, and Seebeck coefficient to be extracted from a single device. Results are also presented from a calibrated thermal atomic force microscopy technique (Ref. 26) which confirm the thermal conductivity measurements. The results to be presented demonstrate ZT and power factors that are enhanced over reference p-SiGe alloys doped at comparable densities and literature values for Si and Ge. The ZT and power factors are also significantly higher than those previously reported for Si/Ge n-type superlattices at room temperature.^{22,23} Finally, analysis of the results indicate a number of parameters that could be improved and optimized to increase the ZT and power factors significantly.

II. MATERIAL DESIGN

The initial suggestions for superlattices on Si substrates to enhance the thermoelectric performance were to use periods consisting of pure Si and pure Ge (Ref. 25), but due to the lattice mismatch, such superlattices require heterolayers below a critical thickness of around 2 nm which significantly reduces the in-plane electrical transport over wider QWs. Such layers are also prone to a high defect density especially from strain relaxation and the breakdown of two-dimensional epitaxy due to the large lattice mismatch. As Ge has higher electrical conductivity and hole mobilities at room temperature ($1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $3 \times 10^{12} \text{ cm}^{-2}$ carrier density)¹² and also higher p-type Seebeck coefficients than Si (Refs. 27 and 28, see Table I for a comparison of thermoelectric properties), a design using Ge QWs was chosen for maximum

TABLE I. A comparison of Si, Ge, Si/Ge, and SiGe thermoelectric parameters from the literature and the present work.

Material	N_A (cm^{-3})	σ (S/m)	α ($\mu\text{V/K}$)	κ ($\text{W m}^{-1}\text{K}^{-1}$)	ZT (300 K)	Power factor ($\text{mW m}^{-1} \text{K}^{-2}$)
p-Si ^a	1.5×10^{19}	11 100	148	148	0.00049	2.43
p-Ge ^b	7.1×10^{18}	30 300	300	59.5	0.014	2.72
p-Si _{0.3} Ge _{0.7} ^{c,d}	1.5×10^{20}	25 000	90	6.3	0.010	1.26
p-Si _{0.188} Ge _{0.812}	6.1×10^{18}	34 900	212 ± 9	38.0 ± 4.1	0.012 ± 0.002	1.57 ± 0.13
p-Si _{0.188} Ge _{0.812}	8.5×10^{18}	23 000	298 ± 3	40.3 ± 8.0	0.019 ± 0.004	2.62 ± 0.04
n-Si/Ge superlattice ^e	1.0×10^{16}	400	-620	12.5	0.004	0.15
n-Si/Ge superlattice ^f	1.8×10^{19}	9800	-297.5	0.87
p-Ge/Si _{0.25} Ge _{0.75}	7.1×10^{18}	77 200	280.0 ± 1.1	19.9 ± 4.7	0.091 ± 0.022	6.03 ± 0.05
p-Ge/Si _{0.25} Ge _{0.75}	7.2×10^{18}	27 900	255.0 ± 3.8	4.0 ± 2.1	0.135 ± 0.074	1.82 ± 0.06

^aReference 28.

^bReference 27.

^cReference 27.

^dReference 32.

^eReference 23.

^fReference 22.

electrical conductivity. The aim was to use the high mobility Ge QWs to produce a high electrical conductivity whilst aiming to have the thermal conductivity dominated by the $\text{Si}_{1-y}\text{Ge}_y$ barriers. To maximize the power factor, modulation doping was chosen to produce the highest possible mobility.^{12,13} As Ge has a 4.2% larger lattice constant than Si, the designs also had to be strain symmetrized where the compressive strain of the Ge QW is balanced by the tensile strain of the $\text{Si}_{1-y}\text{Ge}_y$ barriers, therefore requiring a strain relaxation buffer of an intermediate Ge content as described in Refs. 13 and 29. A self-consistent Poisson-Schrödinger solver was used with the deformation potentials and details provided in Ref. 30 to model the band structure and expected carrier densities. Structures with two different concentrations of Ge in the $\text{Si}_{1-y}\text{Ge}_y$ barriers were produced to investigate the changes in electrical and thermal properties with higher Ge concentration differences between the QWs and barriers. The first design used $\text{Si}_{0.3}\text{Ge}_{0.7}$ barriers on $\text{Si}_{0.2}\text{Ge}_{0.8}$ relaxed buffers whilst the second design used $\text{Si}_{0.4}\text{Ge}_{0.6}$ barriers on $\text{Si}_{0.25}\text{Ge}_{0.75}$ relaxed buffers, both with Ge QWs.

Figure 1 shows the heavy-hole (HH) and light-hole (LH) valence bands for the first design with 9 nm Ge QWs and barriers consisting of 7.5 nm of p- $\text{Si}_{0.3}\text{Ge}_{0.7}$ ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$) with 5.0 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$ spacers all lattice matched to a $\text{Si}_{0.2}\text{Ge}_{0.8}$ relaxed buffer. Also plotted is the carrier density indicating that $\geq 90\%$ of the carriers are in the QWs for this design at 300 K if it is assumed that no segregation or diffusion effects in the growth. Segregation and diffusion effects produce QWs that are effectively wider than the designed values and therefore result in the subband states being lower in energy and closer together in the QW. To first order this should result in a higher carrier density inside the QW, but additional dislocation and interface roughness scattering further complicates the process. The Poisson-Schrödinger solutions (not plotted) also demonstrate that the majority of the carriers in the QWs ($\geq 80\%$) are in the HH1 subband state at 300 K with the remaining carriers in the QW predominantly in the LH1 and HH2 states. The integrated density in each

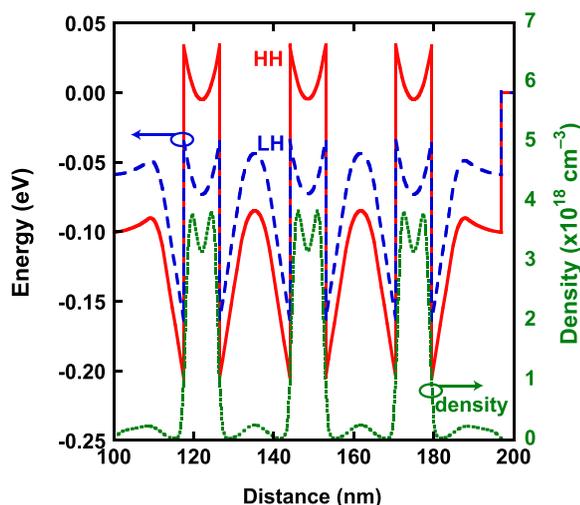


FIG. 1. A self-consistent Poisson-Schrödinger solution showing the HH (red solid line) and LH bands (blue solid line) as a function of vertical distance along with the carrier density (dashed green line) at 300 K.

QW was calculated to be $2.7 \times 10^{13} \text{ cm}^{-2}$ corresponding to $3 \times 10^{19} \text{ cm}^{-3}$.

Previous work undertook a detailed study of this design using a combined approach of the $\mathbf{k}\cdot\mathbf{p}$ theory for the band structure, the Boltzmann equation to determine the carrier transport, Callaway's expression for the thermal conductivity and Monte Carlo modeling to produce the scattering parameters to input to the Boltzmann equation.³¹ The results suggest that a ZT of 0.88 can be achieved in a p-type Ge/SiGe superlattice structure at room temperature provided a threading dislocation density (TDD) of 10^6 cm^{-2} can be achieved.

III. MATERIAL GROWTH

The samples for the work were grown on 100 mm diameter silicon-on-insulator (SOI) substrates consisting of a top Si layer of 340 nm and a SiO_2 layer of 1 μm thickness purchased from SOITEC. A thin Si top layer was chosen to minimize parasitic thermal conducting layers for device measurements. The SiGe heterolayers were grown by low-energy plasma-enhanced chemical vapor deposition (LEPECVD),³³ which has demonstrated the ability to grow high-mobility strained-Ge QWs and multi-QW stacks for optical applications.^{14,34} For the design 1 wafer, a single step buffer of nominally 1 μm $\text{Si}_{0.2}\text{Ge}_{0.8}$ was grown at a rate of 6 nm s^{-1} . For design 2, a two-step (500 nm $\text{Si}_{0.6}\text{Ge}_{0.4}$ at 2 nm s^{-1} , 500 nm $\text{Si}_{0.25}\text{Ge}_{0.75}$ at 6 nm s^{-1}) strain relaxed buffer was grown at 475°C in order to form a virtual substrate for the QWs. While this thin buffer features a higher TDD than that which can be obtained with thick graded buffers,^{13,35} a thick buffer would present a significant parallel thermal conduction channel.

The superlattices themselves were grown at a rate of around 1.4 nm s^{-1} , a growth rate chosen to allow control of layer content and thickness while ensuring that the whole thermoelectric stack can be realized in a reasonable time. Design 1 consisted of 378 repeats of a 9 nm i-Ge QW, 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$ spacer, 7.5 nm p- $\text{Si}_{0.3}\text{Ge}_{0.7}$ supply layer ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$), and a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$ spacer all grown on a $\text{Si}_{0.2}\text{Ge}_{0.8}$ relaxed buffer layer. The surface of the superlattice was capped with a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$ spacer, a 7.5 nm p- $\text{Si}_{0.3}\text{Ge}_{0.7}$ supply layer ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$), a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$ spacer, a 30 nm i- $\text{Si}_{0.2}\text{Ge}_{0.8}$ spacer, and a 4 nm i-Si cap. Design 2 consisted of 378 repeats of a 9 nm i-Ge QW, 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$ spacer, 7.66 nm p- $\text{Si}_{0.4}\text{Ge}_{0.6}$ supply layer ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$), and a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$ spacer all grown on a $\text{Si}_{0.25}\text{Ge}_{0.75}$ relaxed buffer layer. The surface of the superlattice was capped with a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$ spacer, a 7.5 nm p- $\text{Si}_{0.4}\text{Ge}_{0.6}$ supply layer ($N_A = 1 \times 10^{19} \text{ cm}^{-3}$), a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$ spacer, a 30 nm i- $\text{Si}_{0.25}\text{Ge}_{0.75}$ spacer, and a 4 nm i-Si cap. In both cases a 10 μm thick superlattice was chosen so that the active material was approximately 10 times the thickness of the buffer to reduce the electrical and thermal contributions of the buffer and top Si substrate of the SOI.

IV. PHYSICAL CHARACTERIZATION

The inhomogeneity of the growth system means that growth rates vary across a single wafer, and this was used to

produce a range of QW and barrier thicknesses on each sample to allow the thermoelectric properties to be mapped out over a range of QW widths. The wafers were physically characterized by high resolution x-ray diffraction (HRXRD) to investigate thicknesses, strain state and Ge composition laterally averaged over few mm^2 , and transmission electron microscopy (TEM) to determine the QW, barrier, and period thicknesses along with the Ge contents on a very local scale, as well as detailed information on the TDD for samples across the two wafers.

HRXRD measurements were used to characterize the heterolayer composition, strain, thickness, and quality using analysis of line scans along Q_z and reciprocal space maps (RSMs) obtained around the (004) and (224) Bragg reflections. The measurements were performed using a PANalytical X'Pert PRO MRD high-resolution X-ray diffractometer: the system is equipped with a hybrid mirror and 2-bounce asymmetric Ge monochromator for a high-intensity Cu $K\alpha 1$ beam ($\lambda = 0.1540562$ nm). For device processing and thermoelectrical characterization it is particularly important to know the thickness of the multi-QW samples at every point across the 100 mm wafer, which is mapped by taking (004) $\omega - 2\theta$ scans on a 1×1 cm grid. The bending of the substrate, associated with the tensile strain developed during cool down from the deposition temperature,³⁶ is measured from the shift in the ω position of the substrate (004) Bragg peak across the wafer. Defining the wave vector absolute value as $|K| = 2\pi/k$, the longitudinal and perpendicular components of the momentum transfer for a generic reflection are

$$Q_x = 2 \frac{2\pi}{\lambda} \sin(\theta) \sin(\omega - \theta), \quad (4)$$

$$Q_z = 2 \frac{2\pi}{\lambda} \sin(\theta) \cos(\omega - \theta). \quad (5)$$

Figure 2 demonstrates the reciprocal space maps for HRXRD scans of the centre of the design 1 wafer. From the peak positions in the reciprocal space maps we find that the superlattice structure is pseudomorphic to the relaxed buffer of $\text{Si}_{0.18}\text{Ge}_{0.82}$ and is completely strain symmetrized throughout the structure. The clear superlattice peaks in the HRXRD images demonstrate the high quality of the crystal growth. Figure 3 demonstrates a HRXRD radial scan on a sample from the centre of the design 1 wafer. To obtain the Ge composition of the individual layers as well as their thicknesses, the peak positions alone do not contain sufficient information. While the superlattice period can be directly determined from the satellite peak spacing, the thickness ratio can be obtained from the intensity ratio of the satellite peaks. Together with the absolute position of the peaks, mainly influenced by the average composition, the complete information can be derived. To do so, we simulated the (004) intensity profile using a model including, as fit parameters, the thickness of the QW and barrier layers, t_{QW} and t_{B} , and the layer compositions $x_{\text{Ge,QW}}$ and $x_{\text{Ge,B}}$, respectively. Additionally, statistic fluctuations of the layer thicknesses are taken into account as a Gaussian distribution with a width σ_l . These fluctuations lead to additional damping of

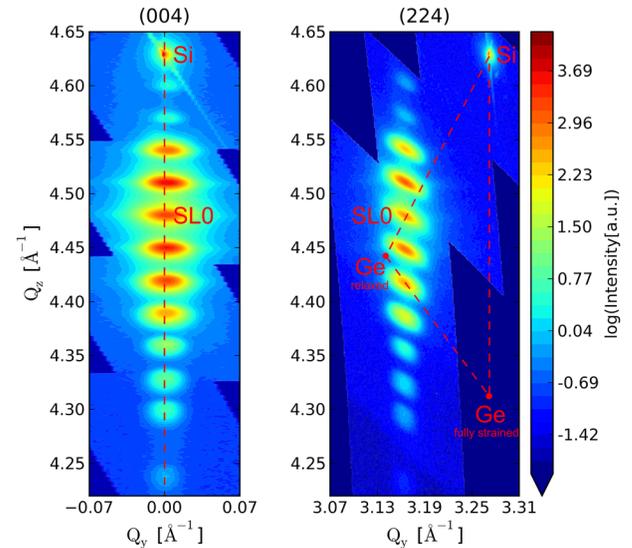


FIG. 2. Reciprocal space maps around the (004) and (224) Si-substrate Bragg peak for the center of the design 1 wafer. In addition to the substrate peak, superlattice oscillations are observed. The dashed line in the (004) map corresponds to the position of the radial scan used for dynamical scattering theory simulations. The dashed triangle in the (224) map corresponds to the relaxation triangle, spanned by the Si and theoretical Ge (fully relaxed and pseudomorphic) Bragg peaks. It can be seen that the 0th-order superlattice peak (SLO) lies exactly on the relaxed line, confirming strain symmetrization.

higher order satellite peaks and to a broadening of the higher order satellites.³⁷ Due to the dislocation network, additional broadening of the peaks occurs in the experiment, which is not captured by our model, so that the peak shapes are not perfectly reproduced. Therefore, we evaluate the integrated intensity as a function of satellite order and fit it with the corresponding data of our simulations.³⁸ The result is shown for the centre of the design 1 wafer in Fig. 4. After performing a series of simulations systematically probing the parameter space, the fine-tuning of the layer thicknesses and Ge compositions is performed in the following way: The superlattice period as well as the average Ge content are fixed to keep the satellite peak positions. The Ge content of the barrier layer $x_{\text{Ge,B}}$ is varied, for each value the ratio of thicknesses t_{QW}

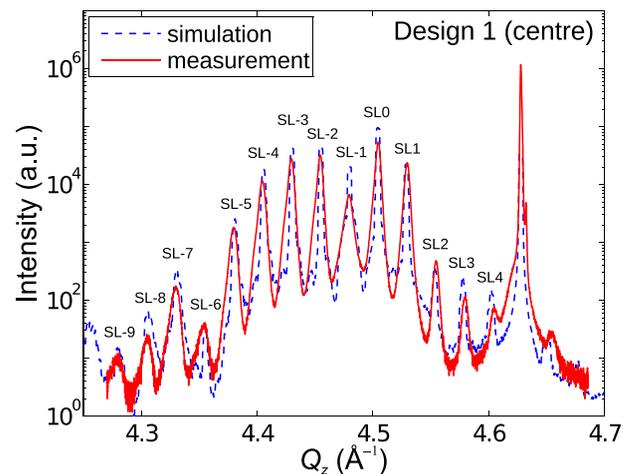


FIG. 3. Radial scan (red) together with fully dynamical Takagi-Taupin simulation (blue) for the parameter set with the best fit to the measurement, for the sample piece at the centre of the design 1 wafer.

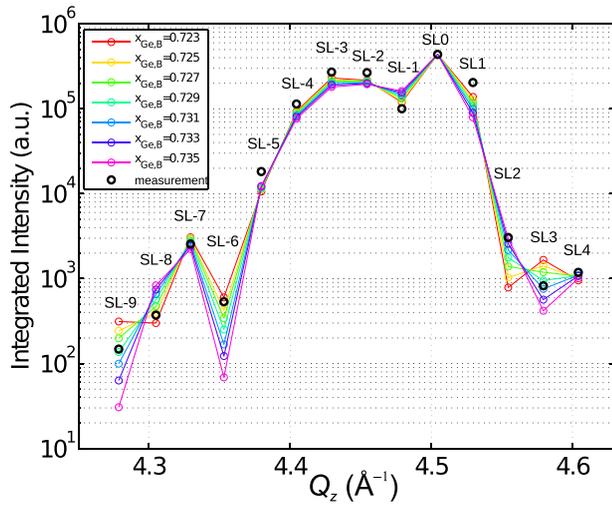


FIG. 4. Intensity of satellite peaks as a function of their position along Q_z for several parameter sets (colored lines and symbols) compared to the experimental data (black circles). The series shows a variation of the barrier composition $x_{\text{Ge,B}}$, the relative thicknesses of barrier and quantum well are adjusted to keep the superlattice period and the average Ge composition constant. All data are normalized to the zero-order satellite peak SL0.

and t_B are adjusted to keep the average Ge composition constant. A series of simulation results show the variation of the relative intensities of the satellite peaks. Especially, the higher order peaks are rather sensitive even to subtle changes in the Ge compositions. The overall best agreement is achieved for $x_{\text{Ge,B}} = 0.729$, with the corresponding values $x_{\text{Ge,QW}} = 0.98$, $t_{\text{QW}} = 9.2$ nm, and $t_B = 16.2$ nm. The uncertainty of the Ge contents corresponds roughly to the step width in $x_{\text{Ge,B}}$ in Fig. 4. In order to match the increasing peak broadening with higher orders, a period fluctuation of Gaussian shape with $\sigma_r = 0.6$ nm was used. The resulting simulation curve together with the measurement is shown in Fig. 3.

Similar characterization was undertaken across all the full wafers to allow an accurate determination of the heterolayer thicknesses and the Ge content for the barriers and buffer layers. Figure 5 shows the thicknesses of the QW, barriers, and period along with the Ge content of the barriers and buffer layers across the design 1 wafer. Whilst the HRXRD modelling and results suggest an error in the Ge contents of the barriers of $\pm < 0.4\%$, the data measured across the wafer in Fig. 5 suggest that accuracy may be closer to $\pm 1\%$. A similar distribution and uncertainty of thicknesses and Ge contents was also obtained by HRXRD maps for design 2 (not shown), and the wafers with reduced numbers of QWs are characterized in Sec. VI.

The SLs were investigated in a Tecnai F30ST TEM operated at 300 kV (0.19 nm point-to-point resolution). The samples were prepared by conventional cross-section preparation (mechanical pre-preparation and Ar-ion etching). TEM was used to provide information about local details not detectable with XRD, such as the origin of surface roughness and short correlation length. The HRXRD quantification of the superlattice period was confirmed by TEM. The layer thicknesses were measured on HRTEM and scanning TEM (STEM) images from the bottom of a QW to the bottom of

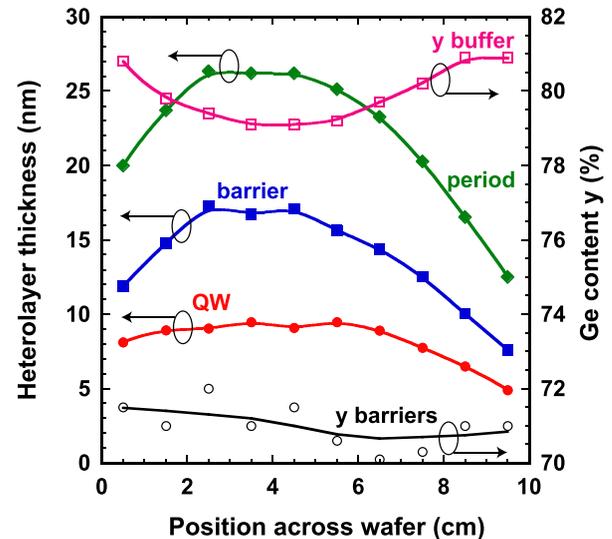


FIG. 5. The thicknesses (solid symbols) and Ge content (open symbols) across the design 1 wafer.

the next or next-but-one overlaying QW. For the determination of the layer thicknesses, intensity profiles along the growth direction averaged parallel to the interfaces were used. The TEM and HRXRD values of the period thicknesses for the samples are generally in good agreement. Within these studies, it was also found that the bottom heterolayers are undulating (the variation of the periodicity is larger than 1 nm, the exact values depend on the specific area) while the top part of the superlattice stack demonstrates significantly flatter interfaces (Fig. 6(a)). These data are in agreement with the X-ray reflectivity results (which are most sensitive to the top part of the structure).

Regarding the material quality, TEM measurements indicated the presence of a rather high TDD, as expected for thin SiGe relaxed buffers. Counting the number of threads on TEM images from a range of samples, TDD densities between 1 and $5 \times 10^9 \text{ cm}^{-2}$ were determined. The dislocations form in the buffer layer and continue to thread into the superlattice layers (Figs. 6(b) and 6(c)). These dislocations give rise to a change of the local heterolayer thicknesses (Fig. 6(d)). The QWs appear to be thinner close to a threading dislocation. This is partly compensated by a larger thickness of the barriers, which tend to flatten the superlattice surface again. Typically, the thickness change is of the order of 3-4 nm over an in-plane length of 30 nm. Similarly to the situation in Si-rich superlattices, the Ge QWs typically provide a rougher surface while Si-rich barriers tend to smoothen the surface again.³⁹

V. DEVICE FABRICATION

Due to the coupling of the important thermoelectric parameters, it is preferable to measure the electrical and thermal properties of the material on a single device test structure. Previous work has demonstrated such a test structure using a van der Pauw geometry device.⁴⁰ This device, however, has a rather complicated thermal path. It is much easier to obtain high accuracy electrical and thermal measurements using Hall bar geometry samples where, provided

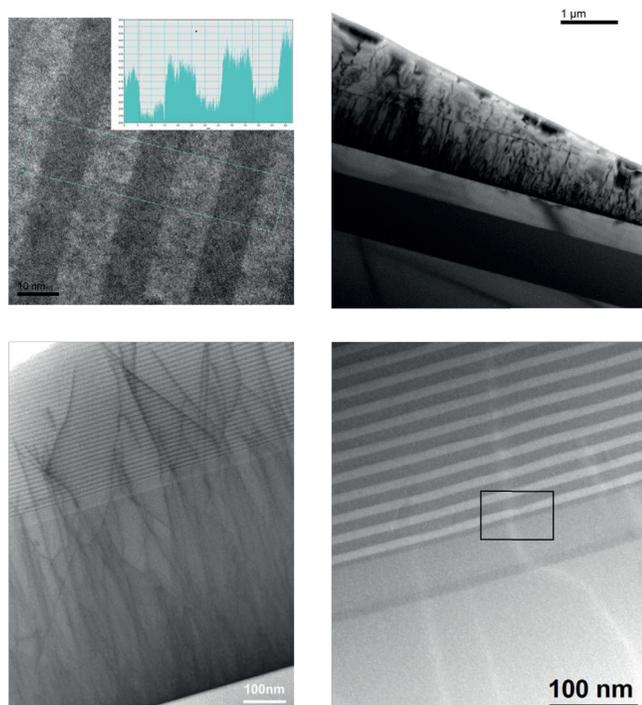


FIG. 6. The layer thickness characterization in the top part of the design 1 superlattice demonstrates a high interface quality and a low roughness on a scale of 50 nm. The faint blue frame in the image indicates where the extracted intensity profile, shown in the inset, was taken. (b) and (c) A high TDD can be recognized in bright field TEM images in the (220) Bragg condition using only the undiffracted beam for imaging. Dislocations are not restricted to the bottom part of the layers but reach the surface with high density. (d) High angle annular dark field scanning transmission electron microscopy image in (110) zone axis orientation shows that in the vicinity of dislocations the QWs (bright contrast) are clearly thinner. This is partly compensated by a corresponding increase in thickness of the next barrier layer.

the correct geometry and length scales are chosen, errors in the measurement of less than 1 part in 10^4 can be achieved.⁴¹

The Hall bar devices were patterned using i-line photolithography and etched using an inductively coupled plasma reactive ion etch (ICP-RIE) process using a mixture of SF_6 and C_4F_8 to obtain a sloping sidewall profile.⁴² This profile allows metal to run continuously down the sides of the mesa. The SOI buried oxide was used as an etch stop. The Al Ohmic contacts were formed after the sputtering of 300 nm of Al followed by an anneal at 400°C which results in low resistivity electrical contacts to the Ge QWs.⁴³ The top of the Hall bar was then coated with 50 nm of inductively coupled plasma-enhanced chemical vapor deposition Si_3N_4 to provide an electrically insulating layer to prevent the heaters and thermometers being electrically shorted. Next the heaters were evaporated using 75 nm of NiCr and patterned by lift-off. Then the thermometers were evaporated using a 20 nm Ti, 100 nm Pt bilayer film. 300 nm thick Al interconnects were sputter deposited and patterned by lift-off to provide interconnects to all the electrical connections required to the Hall bar, heaters, and thermometers. Photolithography was then used to define rectangles on the oxide beside the Hall bar before RIE was used to first etch through the oxide before a SF_6 , and N_2 isotropic dry etch was used to remove the silicon substrate underneath the Hall bar. Figure 7 provides a scanning electron microscope (SEM) image of the

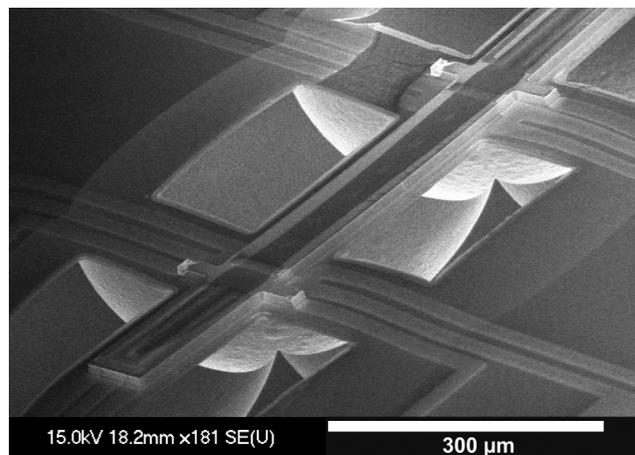


FIG. 7. A SEM image of a free standing Hall bar device with heaters, electrical contacts, and thermometers.

device, and Fig. 8 shows an optical microscope image of the finished devices.

A key issue for the design and placement of the heaters and thermometers on the Hall bar is that the heaters provide a uniform temperature across the full cross section of the Hall bar (i.e., the top and bottom of the superlattice stack are at the same temperature), and whilst the thermometers are measuring the surface temperature, this is the same as the bottom of the superlattice. Finite element analysis using COMSOL was used to solve Fourier's law to allow the heat transport in the Hall bar device to be modeled for a range of powers being applied to the heaters and for a range of thermal conductivities of the superlattice material. The superlattice was modelled as a uniform layer with 3 different thermal conductivities of 2, 10, and $40 \text{ Wm}^{-1} \text{ K}^{-1}$, and in all cases the temperature at the top and bottom of the superlattice stack was identical to within our thermometer measurement accuracy all the way from the hot side thermometer to the cold side thermometer along the Hall bar. The devices were measured in atmospheric pressure as simulations indicated that convection currents should provide an error of 1% or less in the measurement of the temperature along the Hall bar.

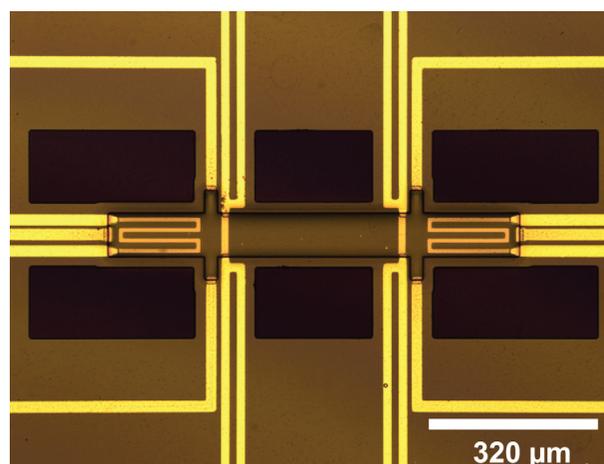


FIG. 8. An optical microscope image of the free standing Hall bar shown in Fig. 7.

VI. ELECTRICAL CHARACTERIZATION

The electrical conductivity was measured using a four terminal dc technique on the Hall bar samples from each wafer to remove any errors from the access resistances on each device. A length to width ratio of 9 and a probe length to width of 2.35 (see Fig. 8) results in a geometrical error in measuring the Hall mobility of less than 1% using these devices.^{44,45} The results as a function of QW width are plotted in Fig. 9. These results need to be compared to the values of p-Ge for $N_A = 10^{19} \text{ cm}^{-3}$ of 33300 S/m and for two reference samples of p-Si_{0.2}Ge_{0.8} doped at the same density which were measured as 34900 S/m and 23000 S/m. The majority of the modulation doped samples has higher electrical conductivities compared to the reference bulk p-SiGe and p-Ge samples. There is a higher level of variability in the electrical results of Fig. 9, and this is believed to be related to the high TDD. Theoretical modeling of these designs indicates that the electrical conductivity decreases significantly for TDDs above 10^6 cm^{-2} whilst the physical characterization indicates TDD over 10^9 cm^{-2} . It is expected that there will be variations in the TDD across a wafer and from sample to sample as the relaxation process and generation of dislocations are effectively random. Also, the TEM and HRXRD results demonstrate the waviness of the bottom QWs from the high TDD levels which will also affect the electrical conductivity and mobility of the QWs.

Figure 10 demonstrates the Hall mobility and the carrier density as a function of the QW width. These devices were again measured using 4 terminal methods on Hall bar samples at magnetic fields of up to $\pm 1 \text{ T}$ to extract the carrier density from the Hall effect. When these results are compared with the later measurements in the paper, the material with higher ZT and power factor results have higher mobilities and lower carrier densities compared to similar samples for design 1. For design 2, however, which has lower carrier density and higher mobilities than design 1, the ZT values are consistently lower than the design 1 results.

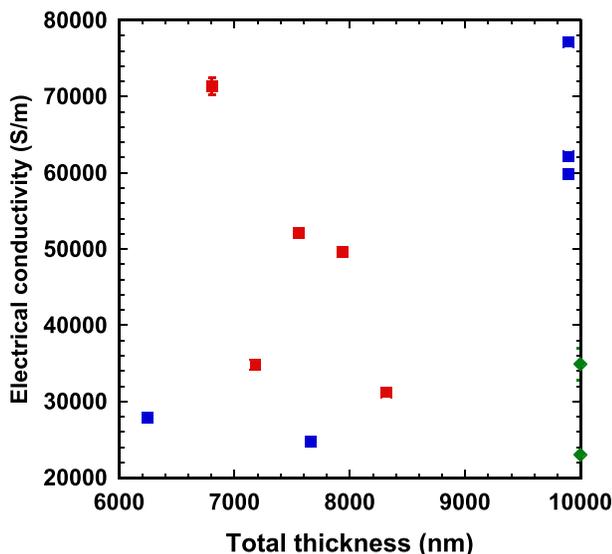


FIG. 9. The electrical conductivity as measured by 4 terminal methods on Hall bar samples versus the QW width of the samples at 300 K. for design 1 (blue squares) and design 2 (red circles).

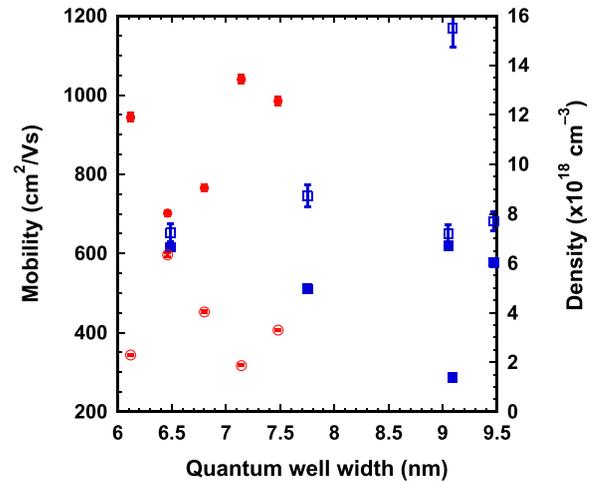


FIG. 10. The Hall mobility (solid symbols) and carrier density (open symbols) versus the QW width of the samples at 300 K for design 1 (blue squares) and design 2 (red circles).

In the full superlattices structure featuring 378 QWs, HRXRD measurements indicate the superlattice stack ranges from 4.5 to $10.2 \mu\text{m}$ thickness in total for the samples tested across the wafer. At 300 K for the lowest electrical conductivity design 1 in Fig. 9, the zero-field ρ_{xx} is only $5.8 \Omega/\text{sq}$, and R_H is $0.28 \Omega/\text{T}$, so the sheet carrier density is $2.2 \times 10^{15} \text{ cm}^{-2}$ (which corresponds to $5.9 \times 10^{12} \text{ cm}^{-2}$ per QW) and the Hall mobility is $480 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Mobility spectrum analysis⁴⁶ was applied to the sample, but the stack of 378 periods is too thick to be able to resolve the mobility peaks due to carriers in the QW and the barriers.

To understand the electrical results more fully, a set of further samples was grown, identical to the design 2 wafer but with 1, 3, 10, and 50 QWs so that the properties of the individual QWs could be understood in addition to the scaling of the electrical properties as the number of QWs was scaled. The mobility as a function of temperature is plotted in Fig. 11, and the results demonstrate that above about 100 K the Hall mobility, μ , decreases with a $\mu \propto T^{-2}$ behaviour typical of optical phonon scattering. The maximum mobilities for all the samples are generally reached in the region of 30 K, and the mobility then decreases with decreasing temperature, indicating ionized impurity scattering.⁴⁷

A key issue is to determine what percentage of the holes is transferred from the supply heterolayers in the barriers into the QWs and the limiting mechanism for the present electrical conductivity. The Hall sheet density per QW is about $1.2 \times 10^{12} \text{ cm}^{-2}$ for the 10 and 50 QW structures, but the 1 and 3 QW structures demonstrated an increase in density with temperature as the dopants were ionized. Analysis of the Shubnikov–de Haas oscillations in the 50 QW sample extracted an average sheet carrier density in each QW of $1.26 \times 10^{12} \text{ cm}^{-2}$. The Hall measured density corresponds to the total density for all quantum wells, and a value of $6.44 \times 10^{13} \text{ cm}^{-2}$ was obtained that corresponds to $1.29 \times 10^{12} \text{ cm}^{-2}$ holes per QW. The extracted effective mass from analysis of the temperature dependence of the Shubnikov–de Haas oscillations was $0.14m_e$ and the Dingle ratio was 4.4 (Fig. 12). An effective mass of $0.135m_e$ is predicted from the analysis in Ref. 48. The extracted Dingle

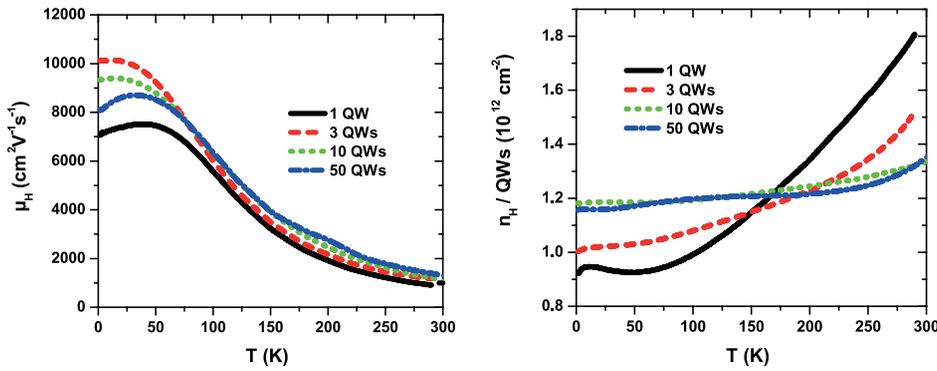


FIG. 11. At high temperatures (>100 K) the Hall mobility (left, measured up to 1 T) decreases with a $\mu \propto T^{-2}$ behaviour typical of optical phonon scattering. Maximum mobilities are generally reached in the region of 30 K, and the mobility then decreases with decreasing temperature, indicating ionized impurity scattering. The Hall sheet density per QW is about $1.2 \times 10^{12} \text{cm}^{-2}$ for the 10 and 50 QW structures, but the 1 and 3 QW structures show some increase in density with temperature as dopants are ionized.

ratio was greater than unity which also suggests that remote impurity scattering or scattering from threading dislocations are the dominant scattering mechanisms rather than local impurity scattering.^{14,49} This suggests that at these low growth temperatures, the dopants have not diffused into the Ge QWs during growth and the samples are modulation doped.

Mobility spectrum analysis was undertaken to determine the ratio of carriers in the QWs and barriers. The mobility spectrum shown in Figs. 13 and 14 demonstrates the excellent fit of the mobility spectrum to the measured magnetoresistance. Using the ρ_{xx} value of $3.87 \text{ k}\Omega/\text{sq}$ at 0 T and the Hall coefficient R_H of $298 \Omega/\text{T}$ measured with a linear fit of ρ_{xy} up to 1 T produces a Hall mobility of only $770 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and a sheet carrier density of $2.1 \times 10^{12} \text{cm}^{-2}$. The peak found by the mobility spectrum analysis produces a QW mobility of $1380 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at a density of $5.8 \times 10^{11} \text{cm}^{-2}$. This analysis indicates that the QWs only account for about half of the total electrical conductivity. Optimized strained Ge QWs^{46,50} have demonstrated Hall mobilities of around $1800 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and channel mobilities of around $3000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$.

The mobility spectrum analysis and low temperature magnetoresistance results therefore suggest that the doping density being used for the modulation doping is presently too high. As the best bulk SiGe results are at carrier densities above $5 \times 10^{19} \text{cm}^{-3}$, the analysis suggests the present superlattice designs require a doping density of at least 1

order of magnitude over the bulk material. Reduction of the doping densities and optimisation of the doping and spacer so that the majority of the carriers reside inside the QW should produce higher hole mobilities with higher electrical conductivities.

VII. THERMAL CHARACTERIZATION

Measuring the thermal properties of materials is significantly more difficult than measuring the electrical properties as most probes of temperature or heat flux will perturb the system being measured. Initial attempts to extract the thermal conductivity used the 3Ω technique, but these resulted in very low values which resulted in anomalously high ZT results. Two independent techniques were therefore used to measure the temperature profile of the devices and to extract the thermal conductivity. The first used calibrated thermometers at either end of the Hall bar. The thermometers were calibrated by immersing the device in perfluoro-1,3-dimethylcyclohexane which is an electrically insulating liquid ($10^{15} \Omega \text{m}$) with a high thermal conductivity to produce an isothermal environment for the calibration. The samples were then placed on a hot plate in contact with a calibrated thermometer, and the temperature varied to obtain the temperature coefficient of resistance (TCR) for each thermometer. A typical TCR for the thermometers was $0.002454 \pm 0.000057 \text{ K}^{-1}$. The liquid was then removed, and the devices characterized as a function of

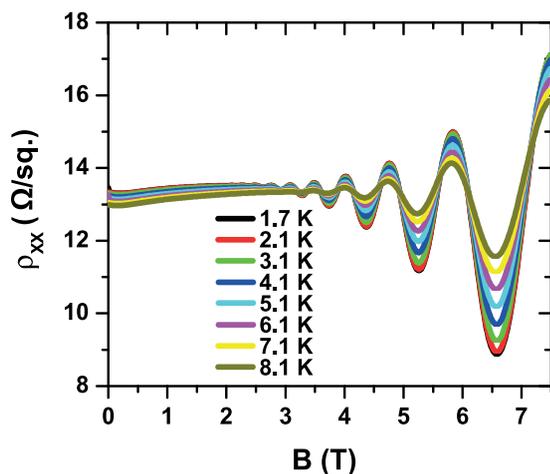


FIG. 12. The Shubnikov de Haas oscillations in the 50 QW sample indicate a sheet carrier density of $1.26 \times 10^{12} \text{cm}^{-2}$ (as compared to the Hall sheet density of $6.44 \times 10^{13} \text{cm}^{-2}$, which corresponds to $1.29 \times 10^{12} \text{cm}^{-2}$ per QW). The effective mass is $0.14 m_e$ and the Dingle ratio is 4.4.

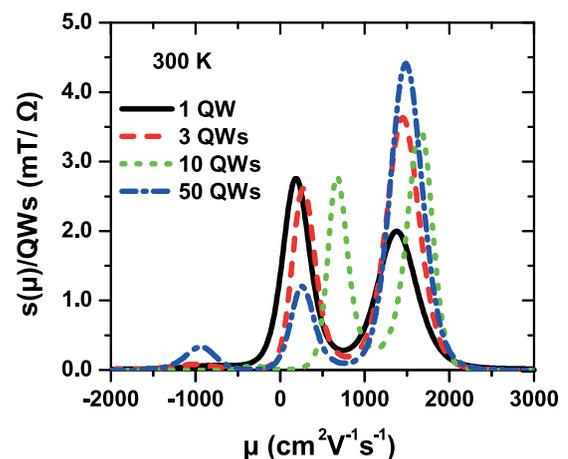


FIG. 13. The mobility spectra at 300 K generally indicate two peaks, corresponding to transport within the QWs and within the doped SiGe layers. The QWs are represented by the peaks at higher mobility, in the region of $1500 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$.

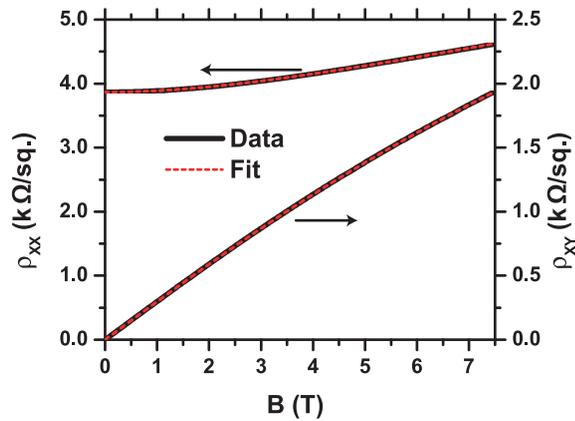


FIG. 14. The magnetoresistance of a structure featuring a single QW; the magnetoresistance calculated from the mobility spectrum in Fig. 13 closely fits the data across the whole range of magnetic field. Positive magnetoresistance (increase of ρ_{xx} with B) is a clear sign of parallel conduction; the decrease in the slope of ρ_{xy} with increasing B is also visible.

heater power. Each device was tested with the heat flow going first in one direction down the Hall bar. The direction of the heat flow was then reversed by using the heater at the opposite end of the Hall bar, and the measurements repeated to provide a self-consistent check that the thermal conductivity was independent of the direction of heat flow along the Hall bar.

For the thermal conductivity measurement, the heat flux, Q , into the central part of the Hall bar is required so that the thermal conductivity can be determined using

$$\kappa = \frac{QL}{wt\Delta T}, \quad (6)$$

in which L is the length of the Hall bar between the thermometers, w is the Hall bar width, and t is the material thickness. To obtain an accurate heat flux, the device was measured as a function of heater power, and the hot and cold side thermometers read. Then the central section of the Hall bar was cut out, and the measurement was repeated so that the parasitic thermal loss down the thermometer contacts and electrical probes could be removed. Finally, the device was simulated using Fourier's law in COMSOL assuming that the superlattice, the buffer, and the SiO_2 supporting membrane had constant thermal conductances so that they could be removed to leave the average thermal conductance of the superlattice film along the Hall bar using the equation

$$\kappa_{SL} = \left[\frac{QL}{\Delta T w} - \kappa_{\text{SiGe}} t_{\text{SiGe}} - \kappa_{\text{Si}} t_{\text{Si}} - \kappa_{\text{SiO}_2} t_{\text{SiO}_2} \right] \frac{1}{t_{SL}}. \quad (7)$$

The thermal conductivity values used for the analysis were $156 \text{ Wm}^{-1} \text{ K}^{-1}$ for Si,⁵¹ $14 \text{ Wm}^{-1} \text{ K}^{-1}$ for SiO_2 ,⁵² and the SiGe buffer values used the measured p- $\text{Si}_{0.188}\text{Ge}_{0.812}$ of $38.0 \text{ Wm}^{-1} \text{ K}^{-1}$. Further details on this technique can be found in Ref. 53.

The second technique used scanning thermal atomic force microscopy (SThAFM), which uses the 4 terminal measurement of a resistance thermometer at the end of a silicon nitride AFM tip to provide a low thermal conductivity temperature probe. The probe is designed to allow measurement of temperature with a spatial resolution below 100 nm,

and the low thermal conductivity and mass of the probe perturbs the temperature measurement by less than 0.2 K.²⁶ The SThAFM thermometers were calibrated using a Johnson noise technique (Ref. 26) which was determined to have a standard deviation of 0.4 K on measuring across the width of one of the Hall bar samples. Figure 15 demonstrates a typical series of 7 scans of $70 \mu\text{m}$ (the AFM system has a maximum scanning field size of $80 \mu\text{m}$) stitched together down one of the Hall bar samples which can be used to determine the ΔT for Seebeck measurements or through fitting with Fourier's equation to determine the thermal conductivity. Alignment marks were etched into the $50 \text{ nm Si}_3\text{N}_4$ surface layer every $50 \mu\text{m}$ along the Hall bar to allow stitching of sufficient accuracy for the present measurements ($<0.5 \mu\text{m}$). The sample in Fig. 15 is one from design 1 which was determined to have a thermal conductivity of $40 \text{ Wm}^{-1} \text{ K}^{-1}$ by SThAFM whilst the calibrated thermometers produced a value of $41.4 \pm 8.2 \text{ Wm}^{-1} \text{ K}^{-1}$.

The Seebeck coefficients were measured at room temperature using heater powers at one end of the Hall bar up to 25 mW which results in ΔT 's down the Hall bar material ranging from 5 to 25 K. A range of powers and therefore ΔT were used, and a least squares fit was used to determine the value. The temperature profile was checked using the SThAFM technique and both techniques resulted in Seebeck coefficients which differed by less than 0.1%. Fig. 16 demonstrates the measured Seebeck coefficient as a function of QW width for samples from wafer designs 1 and 2. The bulk p- $\text{Si}_{0.188}\text{Ge}_{0.812}$ doped at $N_A \sim 6-8 \times 10^{18} \text{ cm}^{-3}$ produced values of 212 ± 9 and $298 \pm 3 \mu\text{V/K}$ whilst bulk p-Si is $148 \mu\text{V/K}$ and bulk p-Ge is $300 \mu\text{V/K}$. The results indicate that the QW samples have Seebeck coefficients comparable to bulk SiGe and Ge values. This suggests that these designs

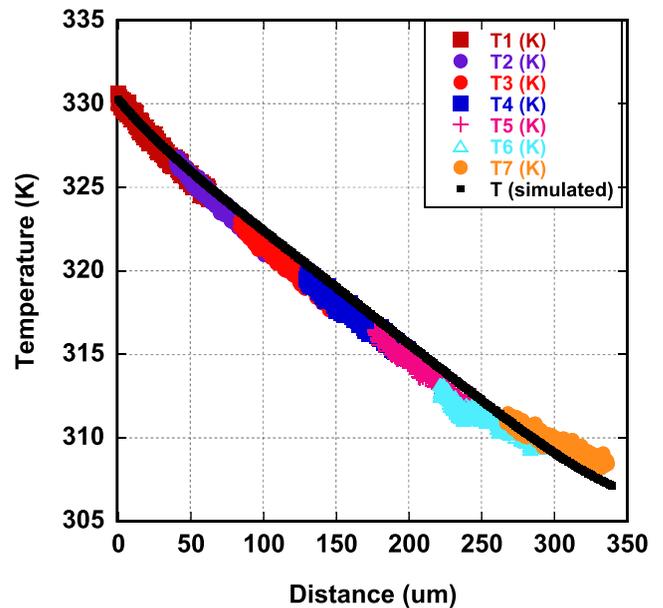


FIG. 15. The temperature measured by the SThAFM as a function of distance from the hot side thermometer on a Hall bar device of bulk p- $\text{Si}_{0.2}\text{Ge}_{0.8}$. As the SThAFM only has a $80 \mu\text{m}$ scan range, 7 scans have been stitched together using holes in the top Si_3N_4 layer as alignment markers. A simulation assuming a $40 \text{ Wm}^{-1} \text{ K}^{-1}$ thermal conductivity for the Hall bar material produces a best fit to the results.

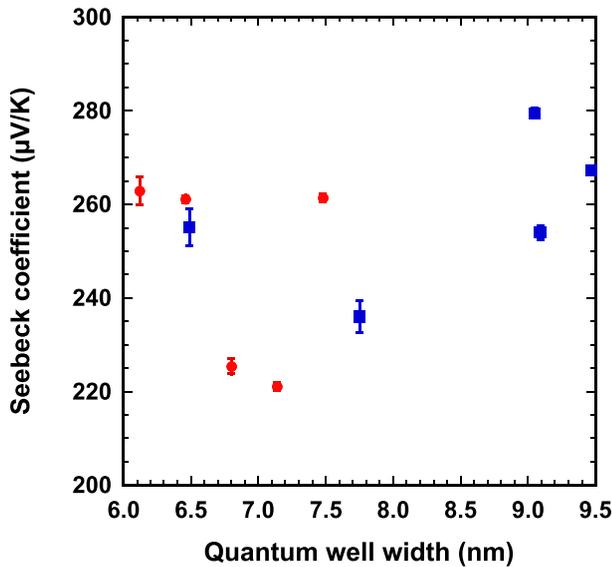


FIG. 16. The Seebeck coefficient versus QW width for design 1 (blue squares) and design 2 (red circles).

are still dominated by carriers in the bulk $\text{Si}_{1-y}\text{Ge}_y$ barrier material, and the QWs are too thick to strongly influence the Seebeck coefficient. Enhancements to the ZT or power factor can only be the result of enhancements to the electrical and thermal conductivities.

Figure 17 demonstrates the thermal conductivity versus quantum well width for the superlattice samples as obtained by the calibrated thermometers. Design 1 shows a clear increase in the thermal conductivity as the QW width was increased. Design 2, however, demonstrates the exact opposite. By replotting the thermal conductivity as a function of electrical conductivity, it becomes clear that the electrical conductivity also has a strong influence on the results (Fig. 18). Ignoring the bulk reference samples, a linear fit can be produced of the form

$$\kappa = \kappa_{ph} + CT\sigma, \quad (8)$$

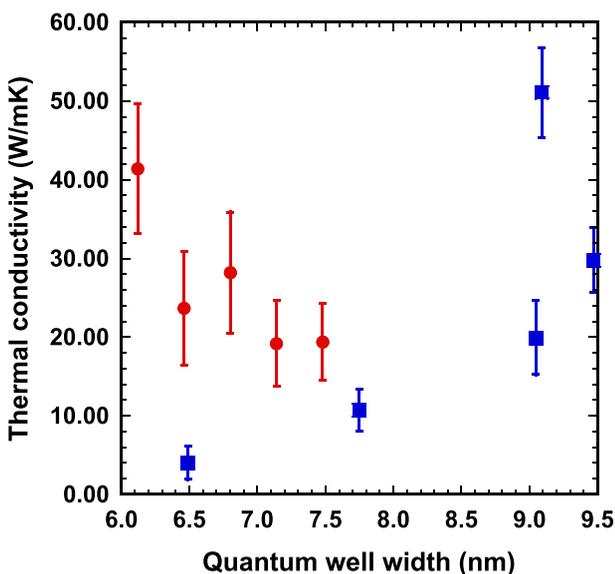


FIG. 17. The thermal conductivity versus QW width for design 1 (blue squares) and design 2 (red circles).

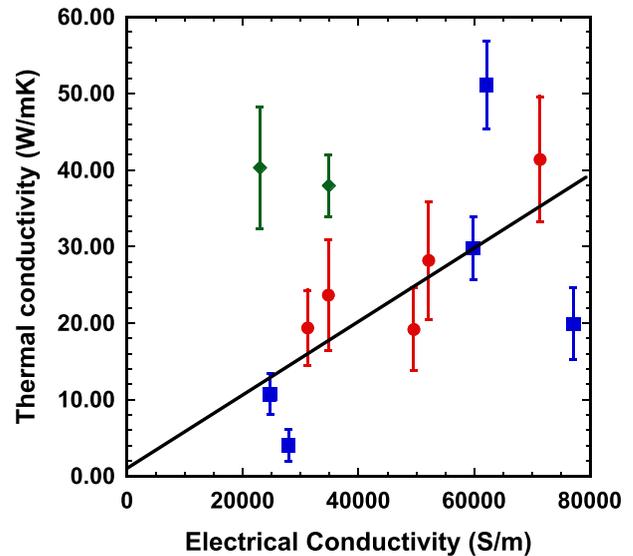


FIG. 18. The thermal conductivity plotted versus the electrical conductivity for each sample. Design 1 (blue squares), design 2 (red circles), and bulk $\text{p-Si}_{0.2}\text{Ge}_{0.8}$ reference samples (green diamonds).

where κ_{ph} is the lattice thermal conductivity and C is a constant which in the Wiedemann–Franz law is the Lorenz number. The present fit to the superlattice data produces a value for C of $1.6 \times 10^{-6} \text{ W}\Omega\text{K}^{-2}$ which is 65 times greater than the Lorenz number indicating that the present thermal conductivity has additional contributions increasing the thermal conductivity. These results combined with the Hall mobility and carrier density results of Fig. 10 suggest that a reduction in the doping density would also produce a reduction in the thermal conductivity. It is clear, however, that there is an additional contribution to the thermal conductivity over the lattice and electronic contributions from the Wiedemann–Franz law. The only possible explanation must be related to the high TDD, and defect density in the samples has an additional contribution to the thermal conductivity.

Design 1 demonstrates lower thermal conductivities than design 2 for the same QW width. This is opposite to what might be expected as it is the device with the lower lattice mismatch (and therefore lower Ge mismatch and acoustic impedance mismatch) that demonstrates the lower thermal conductivity. This suggests that other factors are dominant in the thermal conductivity for such superlattice samples (doping is clearly a factor for these samples) rather than the acoustic impedance mismatch or that provided a sufficient change in Ge content and acoustic impedance can be achieved that this is sufficient for a particular lattice thermal conductivity. Further work is required with more samples to understand this issue fully.

A third issue is the thermal conductivity of the reference bulk $\text{p-Si}_{0.188}\text{Ge}_{0.812}$ samples where the measured thermal conductivities around $40 \text{ Wm}^{-1} \text{ K}^{-1}$ are about a factor of 4.5 higher than the literature values published by Dismukes *et al.* of $7.4 \text{ Wm}^{-1} \text{ K}^{-1}$ for $N_A = 2 \times 10^{20} \text{ cm}^{-3}$.⁷ As the samples in Ref. 7 are more heavily doped than the present samples, the Wiedemann–Franz law and higher doping cannot explain the high thermal conductivity of reference samples in this work. Later analysis of the SiGe samples used in

Ref. 7 indicated that they were poly crystalline and also contained a range of impurities including Cu and other heavy metals.⁵⁴ One conclusion that could therefore be drawn is that these poly crystalline samples demonstrated lower thermal conductivity than the single-crystal samples in this work due to higher levels of phonon and/or hole scattering at grain boundaries and impurities.^{7,32,54} A second possibility is that the high TDD of the present samples grown directly on SOI wafers results in higher thermal conductivity through hole transport along dislocations. Previous work has demonstrated that electrical transport along screw and mixed dislocations can increase leakage currents in resonant tunneling diodes⁵⁵ and Schottky diode devices,⁵⁶ and similar mechanisms are expected in the present samples. Further work and analysis is required to clarify the difference in thermal conductivity measurements between this work at that of Dismukes.^{7,32,54}

VIII. FIGURES OF MERIT AND ANALYSIS

The power factor as a function of QW width is plotted in Fig. 19. The best of these results is higher than the previously reported values for bulk Si, Ge, or SiGe material at comparable carrier densities and significantly higher than the previously reported n-type Si/Ge superlattices at 300 K (see Table I). For design 1, the wider QW samples that also have the higher electrical conductivity demonstrate the highest power factors. For design 1, it is the thinnest QW with the highest electrical conductivity (this sample had the lowest carrier density but the highest mobility from design 1) that demonstrates the highest power factor. This is to be expected since the Seebeck coefficients are not significantly enhanced over bulk material (see Table I and Fig. 16). As the sample with the lowest carrier density had the highest power factor, this is further evidence that the doping in all the samples is too high resulting in reduced figures of merit.

Figure 20 demonstrates the figure of merit ZT as a function of QW width. The large error bars result predominantly from the large error in the measurement of the thermal

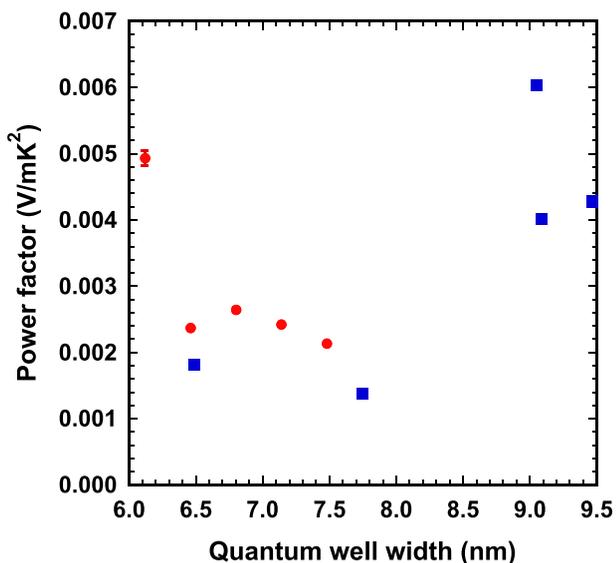


FIG. 19. The power factor as a function of the QW width for design 1 (blue squares) and design 2 (red circles).

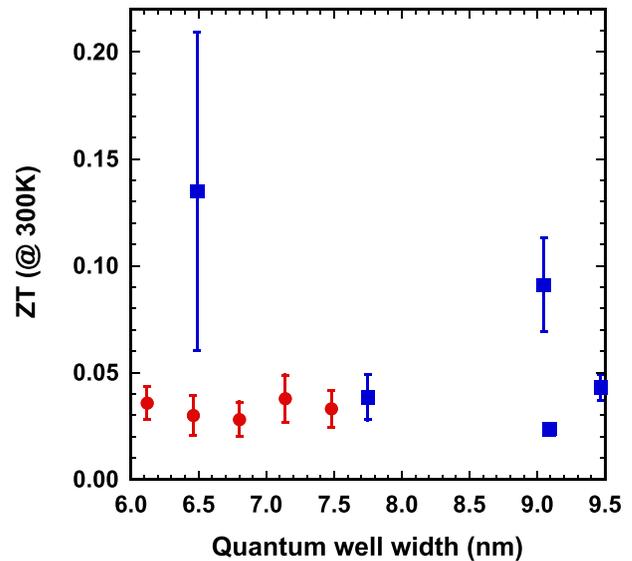


FIG. 20. The figure of merit ZT as a function of the QW width for design 1 (blue squares) and design 2 (red circles).

conductivity especially for the sample with the lowest value of thermal conductivity which is also the sample with the highest ZT . The highest ZT values are both from design 1 suggesting that the higher acoustic mismatch is not important for high ZT at least with the present designs. The two highest ZT values have very different electrical and thermal properties. The first has the highest electrical conductivity but also the highest thermal conductivity whilst the second has the lowest thermal conductivity and a low electrical conductivity too. Both samples had similar mobility values of around 619 and $615 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively, indicating that a significant proportion of the carriers are still in the barriers.

It is clear from all the results that these samples have doping concentrations which are too high to optimize both the electrical and the thermal conductivities. This therefore suggests that the required doping for these 2D designs is at

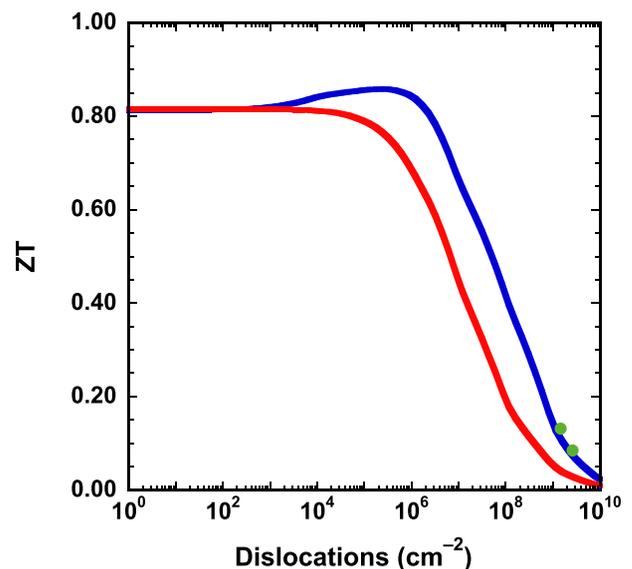


FIG. 21. The figure of merit ZT as theoretically calculated³¹ as a function of TDD. The two green solid symbols are data from design 1 samples.

least 1 order of magnitude less than equivalent bulk 3D material. This is expected to reduce the thermal conductivity by reducing the electrical contribution to the thermal conductivity in the SiGe barriers whilst also increasing the electrical conductivity by improving the number of carriers in the high mobility Ge QWs for the present samples and increasing the Seebeck coefficient. The previous modeling of these designs investigated the value of ZT as a function of TDD.³¹ It is clear that one of the major issues with the present samples is the high TDD values and these have a significant impact on the value of ZT as demonstrated by Fig. 21. The TDD requires a reduction of a factor of at least 100 to achieve useful performance where $ZT > 0.6$ at room temperature. The strain relaxation buffer is one area that does require further optimization to reduce the TDD value. There are other possibilities including SiGe on insulator wafers which would help to reduce the TDD and potentially improve the ZT .

IX. CONCLUSIONS

Thermoelectric results and physical characterization have been presented from two different modulation doped p-Ge QW superlattice designs. The results are the highest reported ZT s for Si-based superlattice designs at room temperature whilst also providing a significant enhancement of the power factor over previously reported results. The best ZT s, whilst superior to previous results in the literature from Si, SiGe, or Ge, are still very modest compared to the best Bi₂Te₃ for room temperature thermoelectrics. Theoretical analysis suggests that the TDD of the strain relaxation buffer is required to be reduced by a factor of 100 before the results become comparable to the materials being used in production today. A second issue is that the ZT is expected to increase for a reduction in the doping density in the superlattices. As the maximum ZT occurs for most bulk materials at $N \geq 5 \times 10^{19} \text{ cm}^{-3}$, the present results indicate that 2D systems require doping densities at least an order of magnitude below their 3D counterparts for the optimum performance. Results on bulk p-Si_{0.188}Ge_{0.812} samples also indicate thermal conductivities about 4.5 times larger than those previously reported.

ACKNOWLEDGMENTS

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